CLAIMS

1. A method of operating a DRAM device in either a high power, full density mode or a low power, half density low mode, comprising:

reordering each row address applied to the DRAM device by making the most significant bit of the row address the least significant bit of a reordered row address, and each of the remaining bits of the row address the next highest order bit of the reordered row address;

when operating in the full density mode, accessing rows of memory cells in an array according to the reordered row address;

when operating in the full density mode, refreshing the memory cells in the array at a first rate;

when operating in the half density mode, accessing rows of memory cells in the array according to the reordered row address, and, when accessing each row of memory cells, also accessing an adjacent row of memory cells;

when operating in the half density mode, refreshing memory cells in the memory array at a second rate that is slower than the first rate; and

when switching from operation in the full density mode to operation in the half density mode, transferring data from each row of the array in which data are stored to the adjacent row of memory cells.

2. The method of claim 1 wherein the act of transferring data from each row of the array to the adjacent row comprises:

activating a word line for the row thereby coupling each of the memory cells in the row to one of a respective pair of complimentary digit lines;

sensing the voltage between each of the complimentary pairs of digit lines using a respective sense amplifier that drives the differential voltage between the complimentary digit lines to a predetermined voltage; and

while each of the sense amplifiers is driving the predetermined voltage between the respective pair of complimentary digit lines, activating a word line for the

adjacent row thereby coupling one of each of the pairs of complimentary digit lines to the respective memory cell in the adjacent row.

3. The method of claim 2 wherein the act of activating a word line comprises activating a word line for an even-numbered row, and wherein the act of activating a word line for a row adjacent the activated word line while each of the sense amplifiers is driving the predetermined voltage between the respective pair of complimentary digit lines comprises activating an odd-numbered word line for a row adjacent the even-numbered row having the activated word line.

4. The method of claim 1 wherein the DRAM device includes a pair of complimentary digit lines for each column of the array, and wherein, when operating in the half density mode, the act of accessing rows of memory cells in the array according to the reordered row address and accessing the adjacent row of memory cells comprises coupling a memory cell in each column of the accessed row of memory cells to the same digit line to which a memory cell in the same column of the adjacent row of memory cells is coupled.

5. The method of claim 1 wherein the DRAM device includes a pair of complimentary digit lines for each column of the array, and wherein, when operating in the half density mode, the act of accessing rows of memory cells in the array according to the reordered row address and accessing the adjacent row of memory cells comprises coupling a memory cell in each column of the accessed row of memory cells to a different digit line from which a memory cell in the same column of the adjacent row of memory cells is coupled.

6. A method of operating a DRAM device, comprising:

reordering each row address applied to the DRAM device by making the most significant bit of the row address the least significant bit of a reordered row address, and each of the remaining bits of the row address the next highest order bit of the reordered row address; and

accessing rows of memory cells in a memory array according to the reordered row address.

7. A method of operating a DRAM device in either a high power, full density mode or a low power, half density mode, comprising:

when operating in the full density mode, refreshing rows of memory cells in an array one-row-at-a-time at a first rate;

when operating in the half density mode, refreshing rows of memory cells in the array two-rows-at-a-time at a second rate that is slower than the first rate; and

when switching from operation in the full density mode to operation in the half density mode, transferring data from each row of the array in which data are stored to another row of memory cells.

8. The method of claim 7 wherein the act of transferring data from each row of the array in which data are stored to another row of memory cells comprises transferring data from each row of the array in which data are stored to a respective adjacent row of memory cells.

9. The method of claim 7 wherein the act of transferring data from each row of the array in which data are stored to another row of memory cells comprises:

activating a word line for the row in which data are stored thereby coupling each of the memory cells in the row to one of a pair of respective complimentary digit lines;

sensing the voltage between each of the pairs of complimentary digit lines using a respective sense amplifier that drives the differential voltage between the complimentary digit lines to a predetermined voltage; and

while each of the sense amplifiers is driving the predetermined voltage between the respective pair of complimentary digit lines, activating a word line for the another row of memory cells thereby coupling one of the digit lines in each of the pairs of complimentary digit lines to the respective memory cell in the another row of memory cells.

10. The method of claim 9 wherein the act of activating a word line for the another row of memory cells thereby coupling one of the digit lines in each of the pairs of complimentary digit lines to the respective memory cell in the another row of memory cells comprises activating a word line for a respective adjacent row of memory cells thereby coupling one of the digit lines in each of the pairs of complimentary digit lines to the respective memory cell in the respective adjacent row of memory cells.

11. The method of claim 7 wherein the act of refreshing rows of memory cells in the array two-rows-at-a-time comprises simultaneously refreshing adjacent rows of memory cells.

12. The method of claim 7 wherein the DRAM device includes a pair of complimentary digit lines for each column of the array, and wherein, when operating in the half density mode, the act of refreshing rows of memory cells in the array two-rows-at-a-time comprises simultaneously coupling a memory cell in each column of one row of memory cells to the same digit line to which a memory cell in the same column of another row of memory cells is coupled.

13. The method of claim 7 wherein the DRAM device includes a pair of complimentary digit lines for each column of the array, and wherein, when operating in the half density mode, the act of refreshing rows of memory cells in the array two-rows-at-a-time comprises simultaneously coupling a memory cell in each column of one row of memory cells to a different digit line from which a memory cell in the same column of another row of memory cells is coupled.

14. A dynamic random access memory ("DRAM") comprising:

an array of memory cells arranged in rows and columns, each row of memory cells having a respective word line that is activated to couple the memory cells in the row to one of a respective pair of complimentary digit lines;

a row decoder coupled to receive a row address and being operable to activate a word line corresponding thereto;

a column decoder coupled to receive a column address and being operable to select a memory cell in a column corresponding thereto;

an input/output control circuit including a sense amplifier for each column of memory cells in the array, the input/output control circuit coupling data between the memory cells in the array and a data bus;

a row address counter coupled to the row decoder, the row address counter being operable to increment by one in a full density mode and to increment by two in a half density mode, the row address counter being operable to generate row addresses corresponding to the count of the row address counter;

a refresh control circuit operable in either a full density mode or a half density mode, the refresh control circuit being operable to cause data to be transferred from memory cells in each row of the array in which data are stored to another row of memory cells when switching from operation in the full density mode to operation in the half density mode, the refresh control circuit further being operable to refresh each row of memory cells selected by a row address from the row address counter in the full density mode and to simultaneously refresh two rows of memory cells selected by a row address from the row address counter in the half density mode; and

a refresh timer operable to control the rate at which the rows of memory cells are refreshed in the full density mode and in the half density mode.

15. The DRAM of claim 14 wherein the row decoder comprises:

an even row address decoder coupled to the word lines for the even-numbered rows of the memory array; and

an odd row address decoder coupled to the word lines for the odd-numbered rows of the memory array.

16. The DRAM of claim 14 wherein the row decoder is operable in the full density mode to reorder each row address applied to the DRAM device by making the most

significant bit of the row address the least significant bit of a reordered row address, and each of the remaining bits of the row address the next highest order bit of the reordered row address, the row addresses generated by the row decoder corresponding to the reordered row addresses.

17. The DRAM of claim 14 wherein, when switching from operation in the full density mode to operation in the half density mode, the refresh control circuit is operable to cause data from each row of memory cells in the array in which data are stored to be transferred to an adjacent row of memory cells.

18. The DRAM of claim 14 wherein the row address counter comprises:

a first counter operable to increment by one responsive to an auto refresh command; and

a second counter operable to increment by one in the full density mode and to increment by two in the half density mode.

19. The DRAM of claim 14 wherein the refresh timer is operable to cause the refresh of rows of memory cells at a first rate in the full density mode and at a second rate in the half density mode, the second rate being slower than the first rate.

20. The DRAM of claim 14 further comprising a mode register that may be externally programmed, the mode register being coupled to the refresh control circuit to permit operation in the half density mode responsive to predetermined mode data being stored in the mode register.

21. The DRAM of claim 14 wherein the DRAM comprises a synchronous DRAM.

22. A dynamic random access memory ("DRAM") comprising:

an array of memory cells arranged in rows and columns, each row of memory cells having a respective word line that is activated to couple the memory cells in the row to one of a respective pair of complimentary digit lines;

a row decoder coupled to receive a row address and being operable to activate a word line corresponding thereto, the row decoder being operable to reorder each row address applied to the DRAM device by making the most significant bit of the row address the least significant bit of a reordered row address, and each of the remaining bits of the row address the next highest order bit of the reordered row address, the row decoder activating word lines for respective rows of memory cells according to the reordered row address;

a column decoder coupled to receive a column address and being operable to select a memory cell in a column corresponding thereto;

an input/output control circuit including a sense amplifier for each column of memory cells in the array, the input/output control circuit coupling data between the memory cells in the array and a data bus;

a row address counter coupled to the row decoder, the row address counter being operable to generate row addresses corresponding to the count of the row address counter;

a refresh control circuit operable in either a full density mode or a half density mode, the refresh control circuit being operable to cause data to be transferred from memory cells in each row of the array in which data are stored to an adjacent row of memory cells when switching from operation in the full density mode to operation in the half density mode, the refresh control circuit further being operable to refresh each row of memory cells selected by a row address from the row address counter in the full density mode and to simultaneously refresh two adjacent rows of memory cells selected by a row address from the row address counter in the half density mode; and

a refresh timer operable to cause the rows of memory cells to be refreshed at a first rate in the full density mode and at a second rate in the half density mode, the second rate being slower than the first rate.

23. The DRAM of claim 22 wherein the row decoder comprises:

an even row address decoder coupled to the word lines for the even-numbered rows of the memory array; and

an odd row address decoder coupled to the word lines for the odd-numbered rows of the memory array.

24. The DRAM of claim 22 wherein the row address counter comprises:

a first counter operable to increment by one responsive to an auto refresh command; and

a second counter operable to increment by one in the full density mode and to increment by two in the half density mode.

25. The DRAM of claim 22 further comprising a mode register that may be externally programmed, the mode register being coupled to the refresh control circuit to permit operation in the half density mode responsive to predetermined mode data being stored in the mode register.

26. The DRAM of claim 22 wherein the DRAM comprises a synchronous DRAM.

27. A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus and adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a dynamic random access memory ("DRAM") device coupled to the processor through the processor bus, the DRAM device comprising:

an array of memory cells arranged in rows and columns, each row of memory cells having a respective word line that is activated to couple the memory cells in the row to one of a respective pair of complimentary digit lines;

a row decoder coupled to receive a row address and being operable to activate a word line corresponding thereto;

a column decoder coupled to receive a column address and being operable to select a memory cell in a column corresponding thereto;

an input/output control circuit including a sense amplifier for each column of memory cells in the array, the input/output control circuit coupling data between the memory cells in the array and a data bus;

a row address counter coupled to the row decoder, the row address counter being operable to increment by one in a full density mode and to increment by two in a half density mode, the row address counter being operable to generate row addresses corresponding to the count of the row address counter;

a refresh control circuit operable in either a full density mode or a half density mode, the refresh control circuit being operable to cause data to be transferred from memory cells in each row of the array in which data are stored to another row of memory cells when switching from operation in the full density mode to operation in the half density mode, the refresh control circuit further being operable to refresh each row of memory cells selected by a row address from the row address counter in the full density mode and to simultaneously refresh two rows of memory cells selected by a row address from the row address counter in the half density mode; and

a refresh timer operable to control the rate at which the rows of memory cells are refreshed in the full density mode and in the half density mode.

28. The computer system of claim 27 wherein the row decoder comprises:

an even row address decoder coupled to the word lines for the even-numbered rows of the memory array; and

an odd row address decoder coupled to the word lines for the odd-numbered rows of the memory array.

29. The computer system of claim 27 wherein the row decoder is operable in the full density mode to reorder each row address applied to the DRAM device by making the most significant bit of the row address the least significant bit of a reordered row address, and each of the remaining bits of the row address the next highest order bit of the reordered row address, the row addresses generated by the row decoder corresponding to the reordered row addresses.

30. The computer system of claim 27 wherein, when switching from operation in the full density mode to operation in the half density mode, the refresh control circuit is operable to cause data from each row of memory cells in the array in which data are stored to be transferred to an adjacent row of memory cells.

31. The computer system of claim 27 wherein the row address counter comprises:

a first counter operable to increment by one responsive to an auto refresh command; and

a second counter operable to increment by one in the full density mode and to increment by two in the half density mode.

32. The computer system of claim 27 wherein the refresh timer is operable to cause the refresh of rows of memory cells at a first rate in the full density mode and at a second rate in the half density mode, the second rate being slower than the first rate.

33. The computer system of claim 27 further comprising a mode register that may be externally programmed, the mode register being coupled to the refresh control circuit to permit operation in the half density mode responsive to predetermined mode data being stored in the mode register.

34. The computer system of claim 27 wherein the DRAM comprises a synchronous DRAM.

35. A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus and adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system; and

a dynamic random access memory ("DRAM") device coupled to the processor through the processor bus, the DRAM device comprising:

an array of memory cells arranged in rows and columns, each row of memory cells having a respective word line that is activated to couple the memory cells in the row to one of a respective pair of complimentary digit lines;

a row decoder coupled to receive a row address and being operable to activate a word line corresponding thereto, the row decoder being operable to reorder each row address applied to the DRAM device by making the most significant bit of the row address the least significant bit of a reordered row address, and each of the remaining bits of the row address the next highest order bit of the reordered row address, the row decoder activating word lines for respective rows of memory cells according to the reordered row address;

a column decoder coupled to receive a column address and being operable to select a memory cell in a column corresponding thereto;

an input/output control circuit including a sense amplifier for each column of memory cells in the array, the input/output control circuit coupling data between memory cells in the array and a data bus;

a row address counter coupled to the row decoder, the row address counter being operable to generate row addresses corresponding to the count of the row address counter;

a refresh control circuit operable in either a full density mode or a half density mode, the refresh control circuit being operable to cause data to be transferred

from memory cells in each row of the array in which data are stored to an adjacent row of memory cells when switching from operation in the full density mode to operation in the half density mode, the refresh control circuit further being operable to refresh each row of memory cells selected by a row address from the row address counter in the full density mode and to simultaneously refresh two adjacent rows of memory cells selected by a row address from the row address counter in the half density mode; and

a refresh timer operable to cause the rows of memory cells to be refreshed at a first rate in the full density mode and at a second rate in the half density mode, the second rate being slower than the first rate.

36. The DRAM of claim 35 wherein the row decoder comprises:

an even row address decoder coupled to the word lines for the even-numbered rows of the memory array; and

an odd row address decoder coupled to the word lines for the odd-numbered rows of the memory array.

37. The computer system of claim 35 wherein the row address counter comprises:

a first counter operable to increment by one responsive to an auto refresh command; and

a second counter operable to increment by one in the full density mode and to increment by two in the half density mode.

38. The computer system of claim 35 further comprising a mode register that may be externally programmed, the mode register being coupled to the refresh control circuit to permit operation in the half density mode responsive to predetermined mode data being stored in the mode register.

39. The computer system of claim 35 wherein the DRAM comprises a synchronous DRAM.